ABSTRACT OF THE DISCLOSURE

A structure for improving electrical performance and interconnection reliability of an integrated circuit in a Wafer Level Packaging (WLP) application comprises an air pad located under an interconnection metal solder pad. Using a low dielectric material such as air underlying the interconnection pad, pad capacitance is reduced, thereby improving the speed of associated electrical signal transitions. By configuring the structure to have interconnection pad supports at only a limited number of pad periphery points, a cured soldered connection can absorb mechanical stresses associated with divergent movement between a connecting wire and the interconnection pad. Such a structure can be manufactured using the steps of: 1) depositing a soluble base material in a cavity on an IC substrate, 2) depositing a metal pad layer on the soluble base layer, and 3) dissolving the soluble base layer, leaving an air gap under the metal pad layer which is supported by the periphery supports.